Design for Testability

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References

- Various materials online, e.g.: web.stanford.edu/class/archive/ee/ee371/ee371.1066/lectures/lect_14.2up.pdf
- This overview of JTAG www.xjtag.com/about-jtag/what-is-jtag/
- The course WWW site:

http://aggregate.org/EE480/

Basic Ideas

- How can a design be made more testable?
  - What features should be included?
  - **Untested things often don't work.**
- How to debug a chip?
- How to handle chips once bugs have been identified?

Functional Test vs. Manufacturing Test

- Functional Testing
  - Is this **design** functionally correct?
  - Huge & expensive effort, largely before fab
  - **If this is bad, every die will be bad**
- Manufacturing Testing
  - Does this particular die work…
    i.e., **can I sell this part?**
  - Effort **repeated for every die**, must be quick
- Same problem could be spotted either place

Functional Test

- Architecture Validation (AV)
  - Active throughout design cycle… for years
  - RTL tests created with design
  - Reuse old tests if possible; make sure old tests survive incremental changes
- First silicon testing of fab'd parts
  - Intense effort to rapidly debug parts
  - "Root cause" > "onion-peeling" > "many rats"

Manufacturing Test

- Can't sell product without testing each unit
  - Slow unit test limits production & sales rate
  - Big investment in Automatic Test Equipment (ATE) to quickly test fab'd parts
- Part binning: often by highest operating frequency… "0 freq." bin makes **keychains** (parts being ranked in lower bins to satisfy higher demand for low-cost parts inspired overclocking, but it is no longer common)

Manufacturing Test Fails Can Kill A Product

- Intel FDIV recall cost ~$500M
  (now Intel places burden on SW developers…
  bugs documented for part revisions)
- Isuzu Trooper bad voltage regulator IC forced recall of ~120,000 cars
- Many "missed windows" of product viability;
  how long to root-cause a problem?
  - Bad test or layout error: 2 person-weeks
  - Marginal/intermittent error: 2 person-months
  - Logic or system-level error: **2 person-years**

Build-In Test & Debug Features

- Use "debug-friendly" layout; for example, put important signals where they can be probed
- Incorporate scan chains to access all memory
- Built-in self-test (BIST)
- Analog probe circuits – even sampling scopes!
- Spare gates – even spare processor cores! (a way to fix a broken chip….)

A Surprising BIST Example

- Modern processors all have "performance registers"
  - Tick count register (high-res. clock)
  - Registers can count various types of events such as cache hits/misses, etc.
- Primary purpose is debugging architecture
  - Also used to plan next generation features
  - Now user-visible, e.g., by Linux PAPI (Performance Application Program Interface)
- Processor chips also have "service processors"

Scan Chains

- **You can't easily debug hidden state…**
  and that's what every latch/flip-flop is
- A scan chain provides an (alternative) path to ***every bit of memory*** on chip:
  - Observable: read any bit (probe access)
  - Controllable: write any bit (set internal state)
- Works even better with flexible clock generators to track-down timing errors

Scan Chains

- The scan chain essentially allows all bits to be accessed as though they were one giant shift register; each bit is a “dual ported” memory
- Probably best known as **JTAG** implementation and the Test Access Port (TAP)
- **Adds ~5% to chip complexity**
- Need to be careful about initial state… **remember only simulators give “X” results**

Other Debugging Aids

- SEM (Scanning Electron Microscope) imaging to reveal fab defects
- E-beam probing to measure voltage on metals
- Remember, chips get bonded face down; you can probe through the back side:
  - LVP (Laser Voltage Probing) shows voltage changes, but not levels
  - TRE (Time Resolved Emission) watches very weak NIR light from switching events

Spare "Happy Gates"?

- Basic cells with grounded inputs, normally doing nothing, perhaps not even powered
- Ever see brightly-colored wires soldered onto chip leads on a circuit board?
  They're ECOs: Engineering Change Orders
- Can actually do similar things on chip:
  - Focused Ion Beam (FIB) can be used to add/remove wires… but not devices

ECOs via FIB

- Can cut or create new wires
- Mostly front side, but can be back side
- **Very expensive!**
  - Repairs one die at a time
  - Typical repair might take 3-5 hours
  - Cost ~$400/hour

It Works! Are We Done?

- Burn-in oven to accelerate infant mortality
  - Part life dramatically decreases with temp.
  - Burn-in at ~125C with ~1.5X normal voltage
- Try to estimate failure rate, time-to-failure
  - Many (complex) failure modes & models
  - Molecular failures include electromigration, breakdown of insulators, etc.
  - Mechanical stresses, solder failure, etc.
  - Soft failures from radiation, etc.
- Want a reasonable lifespan, e.g., ~10 years